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| Serial No: |
| **Final Exam** |
| **Total Time: 3 Hour** |
| **Total Marks: 110** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227 Digital**  **Logic Design** |
| Tuesday 10th May, 2016 |
| **Course Instructor** |
| Dr. Ayub Alvi, Dr. Mewish Hassan,  Mr. Jawad Hassan |

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## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use and mark the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **Fourteen (14)** different printed pages including this **Title page** and an **Rough work page** at the end. There are total of **9 questions**.
5. **Calculator is not allowed**.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. **For each question show your complete method in solution**.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Q-1** | **Q-2** | **Q-3** | **Q-4** | **Q-5** | **Q-6** | **Q-7** | **Q-8** | **Q-9** | **Total** |
| **Total**  **Marks** | **10** | **12** | **10** | **10** | **8** | **10** | **10** | **20** | **20** | **110** |
| **Marks Obtained** |  |  |  |  |  |  |  |  |  |  |

**Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Q 1 [10 = 6+4]**

1. Convert (+49) and (+29) to binary, using the signed-2’s-complement representation and enough digits to accommodate the answer. Perform the binary equivalent of (-29) + (-49). Convert the answer back to decimal and verify that it is correct.
2. The state of a 12-bit register is 1000 1001 0111. What is its content if it represents
3. Three decimal digits in BCD
4. A binary number

**Q2 [12 = 1, 1, 1, 1, 2, 2, 4]**

Table below converts the 4-bit (ABCD) Gray code to 4-bit (WXYZ) Binary code.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D |  | W | X | Y | Z |
| 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |  | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |  | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |  | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |  | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |  | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |  | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 |  | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 |  | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 |  | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |  | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |  | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 |  | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |  | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |  | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 |

1. Write the output W in the form of min-terms
2. Write the output X in the form of max-terms
3. Write the output Y as function ∑ (………)
4. Write the output Y as function π (………)
5. Draw a k-map for output Z and write minimized expression in the form of SoP
6. Draw a k-map for output X and write minimized expression in the form of PoS
7. Draw the **simplified** combinational circuit for all the four outputs (W, X, Y, Z)

**Q 3 [10]**

Implement the following Boolean function F, together with the don’t care conditions D, using no more than TWO NOR gates. Assume that both the normal and complement inputs are available.

F (A,B,C,D) = ∑ (2, 4, 10, 12, 14)

D (A,B,C,D) = ∑ (0, 1, 5, 8)

**Q 4 [10 = 4 + 3 + 3]**

An 8 x 1 multiplexer has inputs A, B, and C connected to the selection inputs S2, S1, and S0 respectively. The data inputs I0 through I7 are as follows:

I1 = I2 = 0; I3 = I7 = 1; I4=I5 = D; and I0 = I6 = D**'**

Construct MUX table, determine the Boolean function that this multiplexer implements and draw MUX diagram.

**Q 5 [8 = 3 + 3 + 2 ]**

Re-design the following combinational circuit using minimum number of components.



1. NOR-NOR gates (two-level)
2. NAND-NAND gates (two level)
3. Decoder and an OR gate

**Q 6 [10 = 4 + 4 + 2]**

Draw symbols of the following components; also write down their characteristics and exitation tables:

1. J-K flip-flop
2. T flip-flop
3. D flip-flop

**Q 7 [ 10 = 4+ 6]**

Implement the following functions by using 8 x 4 ROM.

W ( A, B, C) = ∑ (0, 1, 5, 7)

Y ( A, B, C) = A' B + B' C'

W ( A, B, C) = B' + AC

W ( A, B, C) = ∑ (2, 3, 5)

1. Construct ROM table.
2. Draw ROM Diagram.

**Q 8 [ 20 = 8 + 6 + 6]**

Implement the following functions by using PLA with minimum number of product terms.

**F1 ( w, x, y, z) = ∑ (0, 1, 3, 4, 8, 11, 12, 13, 14, 15)**

**F2 ( w, x, y, z) = ∑ (2, 3, 5, 6, 9, 10, 13, 14)**

**F3 ( w, x, y, z) = ∑ (1, 2, 5, 7, 9, 10, 13, 14)**

**F4 ( w, x, y, z) = ∑ (0, 2, 4, 6, 7, 8, 9, 10)**

1. Select appropriate functions with minimum number of product terms
2. Construct PLA table.
3. Draw PLA Diagram.

**Q 9 [20 = 4+6+6+4]**

Design the smallest possible circuit of a controlled 3 – bit counter (Control input C) using D Flip-Flops.

When input C=0 the counter counts up even numbers: 000 → 010 → 100 → 110 → 000 → etc.

When input C=1 the counter counts down odd numbers: 000− → 111 → 101 → 011 → 001 → 000

**Provide:**

1. State diagram
2. State table
3. Expressions for inputs of D Flip-Flops
4. Circuit Diagram

**Rough Work**